CLAIM AMENDMENTS

Please amend the claims as described below. In accordance with 37 CFR §1.121, a complete listing of all claims in the application is provided below. Notably, the status of each claim is indicated in the parenthetical expression adjacent to the corresponding claim number.

Claims 1 - 27 (**Canceled**).

28. (**Currently Amended**): A semiconductor memory array comprising:

a plurality of memory cells arranged in a matrix of rows and columns, the plurality of memory cells include a first memory cell and a second memory cell, wherein the first and second memory cells each include at least a transistor to constitute the memory cell and wherein the transistor includes:

a source region;

a drain region;

a body region disposed between ~~and adjacent to~~ the source region and the drain region, wherein the body region is electrically floating; and

a gate disposed over the body region; and

wherein each memory cell includes:

a first data state representative of a first charge in the body region; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the source region of the transistor of the first memory cell and the source region of the transistor of the second memory cell are the same region.

29. (**Previously Presented**): The memory array of claim 28 further including a control unit, coupled to the gate and the drain region of the transistor of the first memory cell, to provide control signals to the transistor of the first memory cell, wherein the transistor of the first memory cell, in response to first write control signals , stores the first charge in the body region.

30. (**Previously Presented**): The memory array of claim 29 wherein the first charge is comprised of an accumulation of majority carriers in the body region.

31. (**Previously Presented**): The memory array of claim 30 wherein the majority carriers accumulate in a portion of the body region that is adjacent to the source region.

32. (**Previously Presented**): The memory array of claim 28 further including a control unit, coupled to the gate and the drain region of the transistor of the first memory cell, to provide control signals to the transistor of the first memory cell, wherein the transistor of the first memory cell, in response to second write control signals , stores the second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region.

33. (**Previously Presented**): The memory array of claim 32 wherein the second write control signals include at least first and second signals, each having positive voltages, wherein the first signal is applied to the drain region of the transistor of the first memory cell and the second signal is applied to the gate of the transistor of the first memory cell.

34. (**Previously Presented**): The memory array of claim 28 further including:

a reading unit, coupled to the drain region of the transistor of the first memory cell, to determine the data state of the transistor of the first memory cell;

a control unit, coupled to gate of the transistor of the first memory cell, to provide control signals to the transistor of the first memory cell; and

wherein, in response to a read control signal applied to the gate of the transistor of the first memory cell, the reading unit determines the charge stored in the body region of the transistor of the first memory cell.

35. (**Previously Presented**): The memory array of claim 28 wherein the source regions of the transistors of the first and second memory cells are connected to a fixed voltage.

36. (**Currently Amended**): A semiconductor memory array comprising:

a plurality of memory cells arranged in a matrix of rows and columns, the plurality of memory cell include a first memory cell and a second memory cell, wherein the first and second memory cells each include at least a transistor to constitute the memory cell wherein the transistor includes:

a source region having impurities to provide a first conductivity type;

a drain region having impurities to provide the first conductivity type;

a body region disposed between ~~and adjacent to~~ the source region and the drain region wherein the body region is electrically floating and includes impurities to provide a second conductivity type wherein the second conductivity type is different than the first conductivity type;

a gate disposed over the body region; and

wherein each memory cell includes:

a first data state representative of a first charge in the body region wherein the first charge is substantially provided by impact ionization; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the source region of the transistor of the first memory cell and the source region of the transistor of the second memory cell are the same region.

37. (**Previously Presented**): The memory array of claim 36 further including a control unit, coupled to the gate and drain region of the transistor of the first memory cell, to apply control signals to the transistor of the first memory cell wherein the control signals include first write control signals to accumulate the first charge in the body of the transistor of the first memory cell and second write control signals to provide the second charge in the body region by removing charge from the body region through the source region.

38. (**Previously Presented**): The memory array of claim 37 wherein the first charge is stored in the body region of the transistor of the first memory cell in response to applying a first signal, having a first negative voltage, to the drain region and a second signal, having a second negative voltage, to the gate.

39. (**Previously Presented**): The memory array of claim 38 wherein the transistor of the first memory cell stores at least a substantial portion of the first charge in a portion of the body region of the transistor of the first memory cell that is adjacent to the source region of the transistor of the first memory cell.

40. (**Previously Presented**): The memory array of claim 37 wherein the second write control signals include a first signal, having a first positive voltage, applied to the drain region of the transistor of the first memory cell and a second signal, having a second positive voltage, applied to the gate of the transistor of the first memory cell.

41. (**Previously Presented**): The memory array of claim 40 wherein the source regions of the transistor of the first and second memory cells are connected to a fixed voltage.

42. (**Previously Presented**): The memory array of claim 41 wherein the second charge is stored in the body region in response to removing the first positive voltage from the drain region of the transistor of the first memory cell before removing the second positive voltage from the gate of the transistor of the first memory cell.

43. (**Previously Presented**): The memory array of claim 42 wherein, in response to the first and second positive voltages, the transistor of the first memory cell includes a forward bias current between its body region and its source region.

44. (**Previously Presented**): The memory array of claim 43 wherein the second charge is stored in the body region of the transistor of the first memory cell in response to removing the first positive voltage from the drain region of the transistor of the first memory cell and the second positive voltage from the gate of the transistor of the first memory cell.

45. (**Previously Presented**): The memory array of claim 36 further including:

a reading unit, coupled to the drain region of the transistor of the first memory cell, to determine the data state of the transistor of the first memory cell;

a control unit, coupled to gate of the transistor of the first memory cell, to provide control signals to the transistor of the first memory cell; and

wherein, in response to a read control signal applied to the gate of the transistor of the first memory cell, the reading unit determines the charge stored in the body region of the transistor of the first memory cell.

46. (**Previously Presented**): The memory array of claim 37 wherein the second write control signal include a first signal, having a first positive voltage, applied to the drain region of the transistor of the first memory cell.

47. (**Previously Presented**): The memory array of claim 46 wherein the second charge is stored in the body region in response to removing the first positive voltage from the drain region of the transistor of the first memory cell before removing the second positive voltage from the gate of the transistor of the first memory cell.

48. (**Previously Presented**): The memory array of claim 47 wherein, in response to the first and second positive voltages, the transistor of the first memory cell includes a forward bias current between its body region and its source region.

49. (**Previously Presented**): The memory array of claim 48 wherein the second charge is stored in the body region of the transistor of the first memory cell in response to removing the first positive voltage from the drain region of the transistor of the first memory cell and wherein the source regions of the transistors of the first and second memory cells are connected to a fixed voltage.

50. (**Currently Amended**): A semiconductor memory array comprising:

a plurality of memory cells, arranged in a matrix of rows and columns, including a first memory cell and a second memory cell, wherein the first and second memory cells each include at least a transistor to constitute the memory cell wherein the transistor includes:

a source region having impurities to provide a first conductivity type;

a drain region having impurities to provide the first conductivity type;

a body region disposed between ~~and adjacent to~~ the source region and the drain region wherein the body region is electrically floating and includes

impurities to provide a second conductivity type wherein the second conductivity type is different than the first conductivity type;

a gate spaced apart from, and capacitively coupled to, the body region; and

wherein each memory cell includes:

a first data state representative of a first charge in the body; and

a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region; and

wherein the source region of the transistor of the first memory cell and the source region of the transistor of the second memory cell are the same source region.

51. (**Previously Presented**): The memory array of claim 50 further including a control unit, coupled to the transistor of the first memory cell, to control the data state of the transistor of the first memory cell wherein, in response to a first voltage applied to the drain region of the transistor of the first memory cell and a second voltage applied to the gate of the transistor of the first memory cell, the first charge is removed from the body region of the transistor of the first memory cell through its source region.

52. (**Previously Presented**): The memory array of claim 51 wherein the control unit, in response to removing the first voltage from the drain region of the transistor of the first memory cell before removing the second voltage from the gate of the transistor of the first memory cell, causes the second charge to be stored in the body region of the transistor of the first memory cell.

53. (**Previously Presented**): The memory array of claim 51 wherein the control unit, in response to applying ground to the drain region of the transistor of the first memory cell before removing the second voltage from the gate of the transistor of the first memory cell, causes the second charge to be stored in the body region of the transistor of the first memory cell.

54. (**Previously Presented**): The memory array of claim 51 wherein the control unit, in response to applying a third voltage to the drain region of the transistor of the first memory cell before applying a fourth voltage to the gate of the transistor of the first memory cell, causes the transistor of the first memory cell to store the second charge in its body region.

55. (**Previously Presented**): The memory array of claim 51 wherein the transistor of the first memory cell stores the first charge in a portion of its body region that is adjacent to its source region.

56. (**Previously Presented**): The memory array of claim 51 further including a control unit, coupled to the gate and the drain region of the transistor of the first memory cell, to apply control signals to transistor of the first memory cell wherein:

in response to first write control signals , the transistor of the first memory cell generates and stores the first charge in the body region; and

in response to second write control signals , the transistor of the first memory cell generates and stores the second charge in the body region wherein the transistor of the

first memory cell generates the second charge by removing charge from its body region through its source region; and

wherein the first and second write control signals each include a plurality of signals.

57. (**Previously Presented**): The memory array of claim 56 wherein the first write control signals include a first signal having a first negative voltage to the drain and a second signal having a second negative voltage to the gate and wherein, in response to the first and second negative voltages, the first charge is stored in the body region of the transistor of the first memory cell.

58. (**Previously Presented**): The memory array of claim 57 wherein the transistor of the first memory cell stores the first charge in a portion of the body region of the transistor of the first memory cell that is adjacent to the source region of the transistor of the first memory cell.

59. (**Previously Presented**): The memory array of claim 56 wherein the second write control signals include a first signal having a first positive voltage applied to the drain region and a second signal having a second positive voltage applied to the gate.

60. (**Previously Presented**): The memory array of claim 59 wherein the second charge is stored in the body region in response to removing the first positive voltage

from the drain region of the transistor of the first memory cell before removing the second positive voltage from the gate of the transistor of the first memory cell.

61. (**Previously Presented**): The memory array of claim 59 wherein, in response to the first and second positive voltages, the transistor of the first memory cell includes a forward bias current between its body region and the source region.

62. (**Previously Presented**): The memory array of claim 61 wherein the second charge is stored in the body region of the transistor of the first memory cell in response to removing the first positive voltage from the drain region of the transistor of the first memory cell and the second positive voltage from the gate of the transistor of the first memory cell.

63. (**Previously Presented**): The memory array of claim 50 further including:

a reading unit, coupled to the drain region of the transistor of the first memory cell, to determine the data state of the transistor of the first memory cell;

a control unit, coupled to gate of the transistor of the first memory cell, to provide control signals to the transistor of the first memory cell; and

wherein, in response to a read control signal applied to the gate of the transistor of the first memory cell, the reading unit determines the charge stored in the body region of the transistor of the first memory cell.